IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First Named Inventor	:	KokHoe Chia et al.	Group Art Unit: 2188
Appln. No.	:	10/664,611	Examiner: C. E. Walter
Filed	:	September 18, 2003	
For	:	METHOD AND APPARATUS FOR MANAGING BUFFER RANDOM ACCESS MEMORY	
Docket No.	:	S104.12-0040/STL 11343	

BRIEF FOR APPELLANT

FILED ELECTRONICALLY ON SEPTEMBER 27, 2006

Sir:

This is a Brief in an appeal from an Office Action dated April 4, 2006 in which claims 15-17 were finally rejected. The appellants respectfully submit that claims 15-17 are allowable, and request that the Board reverse the rejection of claims 15-17 and find that claims 15-17 are in condition for allowance.

Contents

REAL PARTY IN INTEREST

Seagate Technology LLC, a corporation organized under the laws of the state of Delaware, and having offices at 920 Disc Drive, Scotts Valley, CA 95066, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the patent application and recorded on Reel 014565, frame 0461.

NO RELATED APPEALS OR INTERFERENCES

There are no known related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF THE CLAIMS

Claims 1-14 were originally presented. Claims 1, 4, 6, 7, 9, 12 and 14 were amended, claims 3 and 11 were canceled, and new claims 15-17 were added with an Amendment filed on January 23, 2006. In the Final Office Action mailed on April 4, 2006, claims 1, 2, 4-10 and 12-17 were allowed, and claims 15-17 were rejected. Claims 15-17 currently stand rejected, while claims 1, 4, 6, 7, 9, 12 and 14 stand allowed. Thus, rejected claims 15-17 are appealed herein.

STATUS OF AMENDMENTS

No amendments have been filed after the final rejection. A Pre-Appeal Brief Request for Review was filed after the final rejection, and has been acted on by a Panel which instructed that the application should proceed to the Board of Patent Appeals and Interferences.

SUMMARY OF CLAIMED SUBJECT MATTER

1. Introduction

The claimed subject matter relates to methods of managing a buffer random access memory. In particular, the claimed subject matter pertains to methods of managing a buffer random access

memory having a first portion allocated for a defect table and a second portion allocated for data caching.

2. Brief Background

In conventional mass storage devices, such as disc drive data storage systems, media defect information is recorded in a defect table that is stored on the recording medium. In a disc drive, the defect table is typically stored in the reserved tracks of the recording medium. Conventionally the defect table has been of a fixed, predetermined sized, length and/or capacity.

The defect table indicates unreliable portions of the recording medium. During production of the mass storage device, the device is tested to determine which portions, if any, of the recording medium are not sufficiently reliable for writing and reading of a data. The address of each of the unreliable portions is stored on the recording medium in the defect table. When the mass storage device is running, the defect table is loaded into buffer random access memory (RAM), provided by a volatile memory device, that is also shared with interface transfer functions for the purpose of data caching.

Typically, larger defect tables for a mass storage device require more buffer (RAM) space. For a given quantity of RAM, this results in less buffer space being available for data caching. A typical disc drive type mass storage device with 80 gigabytes (GB) capacity would require not less than 64 kilobyte (KB) of buffer RAM to be reserved for defect table purposes. The size of the defect table is usually fixed across all disc drives of a particular type with different numbers of headers. A larger defect table size is usually required to insure that defects can be recorded, while at the same time meeting production yield requirements for the particular type of drive. Generally, production yield requirements include having a minimum number of storage devices fail due to insufficient defect table size.

For disc drive type mass storage device with more than 80 GB capacity, such as the 240 GB capacity drives, buffer RAM size the defect table may be as much as three times the buffer RAM size required for drives having less than 80 GB capacity. Thus, these drives may require that as much as 192 KB of buffer RAM be reserved for the defect table. This provides a

significant impact to the performance of low-cost drives that use smaller sized buffer RAM. A method of reducing the portion of the buffer RAM occupied by the defect table, without increasing the number of mass storage devices that fail certification testing due to insufficient defect table storage capacity, would therefore be a significant improvement, particularly for low-cost disc drive type mass storage devices.

3. The Claimed Subject Matter

Independent claim 15 is directed to a method of managing a buffer random access memory (251). The buffer random access memory has a first portion (253) allocated for a defect table and a second portion (254) allocated for data caching. As claimed, the method includes the step of determining (410) actual memory space of the first portion of the buffer random access memory which is actually occupied by the defect table in order to identify unused memory space of the first portion. Then, the method includes the step of reallocating (420) the unused memory space of the first portion of the buffer random access memory for use in data caching. This method is shown particularly in FIG. 4, but is also described generally with reference to FIGS. 2, 3-1, 3-2, 5-1 and 5-2 for example. This method is described throughout the application, but particularly between page 5, line 21 and page 8, line 18.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 15-17 are unpatentable under 35 U.S.C. §102(b) over U.S. Patent No. 6,336,202 B1 issued to Tsuchimoto et al. (hereafter referred to as "Tsuchimoto").

ARGUMENT

1. Claims 15-17 Are Allowable Over Tsuchimoto

In the Final Office Action mailed April 4, 2006, claims 15-17 were rejected under 35 U.S.C. §102(b) as being anticipated by Tsuchimoto. The Examiner's rejection is respectfully traversed, and it is also respectfully requested that the Board reverse the Examiner's rejection of independent claim 15, as well as the rejection of the corresponding dependent claims 16 and 17.

A. Independent Claim 15

Independent claim 15 recites a method of managing a buffer random access memory having a first portion allocated for a defect table and a second portion allocated for data caching. The method includes the step of "determining actual memory space of the first portion of the buffer random access memory which is actually occupied by the defect table in order to identify unused memory space of the first portion." The method then includes the step of "reallocating the unused memory space of the first portion of the buffer random access memory for use in data caching."

B. Tsuchimoto Does Not Anticipate Claims 15-17

As was argued in the Amendment filed on January 23, 2006, Tsuchimoto fail to teach or suggest either of two claim limitations found in independent claim 15, and thus there is an omission of essential elements to establish a prima facie rejection. These omissions were discussed on pages 8 and 9 of the Amendment filed on January 23, 2006.

i. The Step of Determining Actual Memory Space is Not Anticipated

In support of the rejection of independent claim 15 in the Final Office Action mailed on April 4, 2006, the Office Action stated that Tsuchimoto teaches "determining actual memory space of the first portion of the buffer random access memory occupied by the defect table to identify unused memory space of the first portion." To support this position, the Office Action further stated that the controller as illustrated in Fig. 1 of Tsuchimoto "must inherently make a determination which data in the RAM is the defect table and which area in the RAM is for data caching in order for Tsuchimoto's system to work." Tsuchimoto does not support an interpretation which satisfies this limitation of claim 15, and thus the teachings of Tsuchimoto do not support this assertion. Accordingly, there is no basis to support the rejection under 35 U.S.C. §102(b), as a method step required in claim 15 is missing in this prior art reference.

As discussed in the background of the present application, conventionally the size of the

defect table has typically been fixed across all disc drives of a particular type with different numbers of headers. A larger defect table size has usually been required to insure that defects can be recorded, while at the same time meeting production yield requirements for the particular type of drive. Generally, production yield requirements include having a minimum number of storage devices fail due to insufficient defect table size. As a result, on some drives, the defect table will be larger than necessary. Please see the application, page 1, lines 23-32. There is no teaching by Tsuchimoto to conclude that the system disclosed by that reference operates any differently than in this conventional manner. Consistent with this, admittedly, the Tsuchimoto system would likely determine which data in the RAM is allocated for the defect table and which area in the RAM is allocated for data caching. It does not follow, however, that in order to work the Tsuchimoto system must inherently determine actual memory space of the first portion (i.e., the portion defined in the preamble of claim 15 as being allocated for the defect table) of the buffer random access memory which is actually occupied by the defect table to identify unused memory space of the first portion. Tsuchimoto simply does not provide such a teaching. Lacking such a teaching in the reference itself, interpreting Tsuchimoto in this manner in view of the teachings of the present application represents impermissible hindsight. Lacking a specific teaching of this claim limitation, claims 15-17 cannot be anticipated by Tsuchimoto.

ii. The Step of Reallocating the Unused Memory Space is Not Anticipated

Also in support of the rejection of independent claim 15, the Office Action stated that Tsuchimoto teaches "reallocating the unused memory space of the first portion of the buffer random access memory for use in data caching [*sic*] (the remaining memory area in the RAM, not being used to store the variable sized defect table can now be used (i.e., allocated) for data caching purposes." In support of this assertion, the Office Action referred to col. 5, lines 57-67 of Tsuchimoto, and stated that "Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of RAM in the controller." The Office Action then asserts that "[t]he remaining area of the RAM is now allocated for data caching purposes as described at col. 3, lines 20-25." These assertions are also not supported by the teachings of Tsuchimoto.

First, Tsuchimoto provides no actual teaching of reallocating unused memory space of the first portion of the random access memory for use in data caching. Even if the remaining memory area in the RAM, which is not being used to store the defect table can be used for data caching purposes as asserted in the Office Action, the mere fact that it can be used in this manner does not provide a teaching of such a reallocation use. The further statement in the Office Action that "[t]he remaining area of the RAM is now allocated for data caching purposes as described at col. 3, lines 20-25" is not in fact supported by that portion of Tsuchimoto or elsewhere.

Second, the fact that Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of RAM in the controller is not in and of itself a teaching of the recited reallocating limitation. For example, minimization of defect map sizes can be used to reduce the original RAM allocated for the defect table, while leaving this original RAM allocation fixed across all disc drives of a particular type. Regardless, Tsuchimoto provides no specific teaching or suggestion of the reallocating step recited in independent claim 15, and thus cannot anticipate or render obvious claims 15-17.

Section 3 of the Office Action also provided additional analysis regarding Tsuchimoto's teaching of a reassign table at col. 6, lines 43-65 at col. 7, lines 6-26. The Office Action pointed out that the reassign table can be produced either before or after logical formatting, and that if the table is modified, the amount of memory required to store the information will change, resulting in a change in the amount of memory remaining in the RAM for caching purposes. The Office Action concluded that "[w]hen the table is rewritten, the system will automatically reallocate memory in the RAM based on the determination of how much memory is available within the RAM." (Emphasis added). It is again emphasized that Tsuchimoto in fact provides no such teaching of reallocation. The fact that the table can be modified after logical formatting, changing the actual memory requirements of the table, does not in and of itself lead to the conclusion that RAM allocated for the table will be reallocated for use in data caching. For example, the memory allocated for the table in Tsuchimoto could be sufficiently large to allow for changes to the defect table. While Tsuchimoto is not clear on this issue, it is clear that Tsuchimoto provide no teaching or suggestion of the reallocation step of independent claim 15.

Since Tsuchimoto does not anticipate each and every element of claims 15-17, Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) be reversed by the Board.

2. Conclusion : Claims 15-17 Should Be Allowed

In conclusion, the Appellants respectfully submit that claims 15-17 are allowable over the cited reference for at least the reasons laid out above. Thus, the Appellants respectfully request that the Board reverse the rejections of claims 15-17 and find the claims in condition for allowance. The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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Appendix A: Claims On Appeal

15. A method of managing a buffer random access memory, the buffer random access memory having a first portion allocated for a defect table and a second portion allocated for data caching, the method comprising:

determining actual memory space of the first portion of the buffer random access memory which is actually occupied by the defect table in order to identify unused memory space of the first portion; and

reallocating the unused memory space of the first portion of the buffer random access memory for use in data caching.

16. A controller configured to implement the method of claim 15.

17. A mass storage device comprising the controller of claim 16.

Appendix B: Evidence Appendix

There is no known evidence submitted pursuant to 37 CFR §§ 1.130, 1.131 or 1.132 or other evidence entered by the Examiner.

Appendix C: Related Proceedings Appendix

There are no known related appeals or interferences regarding the present appeal.